

R-INTERFACE CHANNELIZERS INCREASE AGILITY AND EFFICIENCY IN THE MULTICHANNEL DOWNCONVERSION PROCESS

General Description

Wideband software defined radio architectures are used for infrastructure systems, including cellular base stations, tactical communications gateways, and satellite communications hubs, where dozens or even hundreds of simultaneous carrier channels may be active at any one time. Wideband architectures are also useful in a number of niche applications for military and civil defense, including signals intelligence and electronic warfare.

Digital Down Converters (DDC) are one of the essential functions of Software-Defined radio applications. The DDC function can be integrated as an ASIC chip or as an FPGA-based IP core. The inherent flexibility of software radio applications make them require most of the times FPGA-based architecture.

Wideband communication systems such as commercial wireless base station, monitoring systems, military radio network usually need to process a large number of channels with flexibility on channel spacing and bandwidth.

The basic DDC function implements three front end functions which are channel frequency translation, channel separation, and channel decimation. The frequency translation is implemented using a Direct Digital Synthesis (DDS), while channel filtering performs channels separation and decimation.

The basic DDC structure is flexible but very resource consuming. As an example a 70dB SFDR DDC from Xilinx LogiCore consume 1500 slices, yielding as a maximum to the implementation of a dozen DDCs on a midsize FPGA. On the other side parallel FFT based channelizer are efficient in term of silicium area but yield to very few agility.

R-Interface patents a very efficient and agile FPGA-based digital channelizer. The solution allows high complexity gains compare to traditional DDC (Digital Down Conversion) structure while keeping the flexibility.

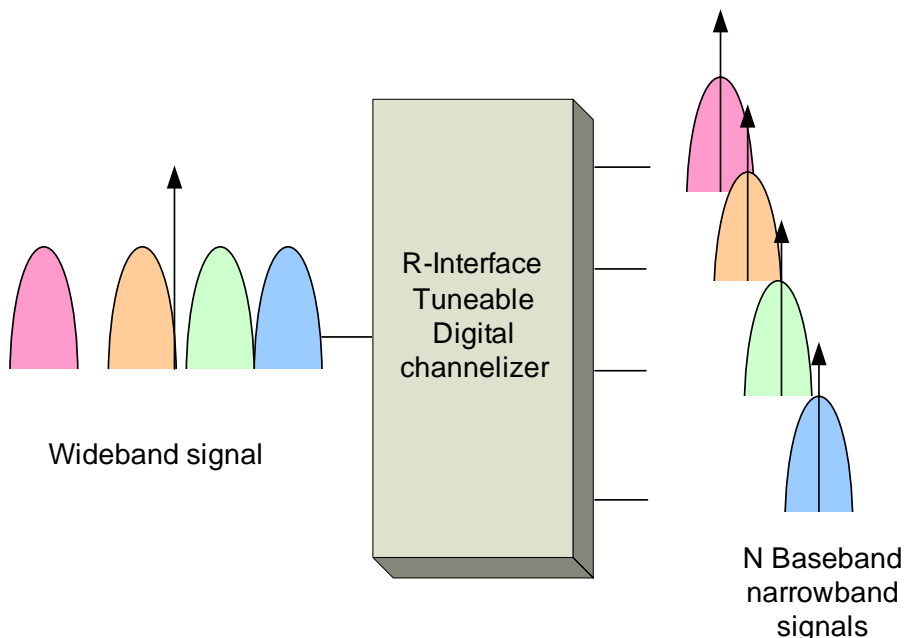


Figure 1

- Number of channels : 8 to 1024 channels

- Targets: Xilinx, Altera FPGAs

R-Interface tunable channelizer

R-Interface proposes a family of channelizer based on building blocks concept to adapt your needs and optimized your silicon resource.

Accepting real and complex data input at rate up to 160MHz, the R-Interface core is able to down convert $N = 8$ to 1024 channels.

This version proposes an optimal configuration in order to be very agile; it allows to down convert the input signal and to select several channels with the same agility than the DDC in term of frequency selection.

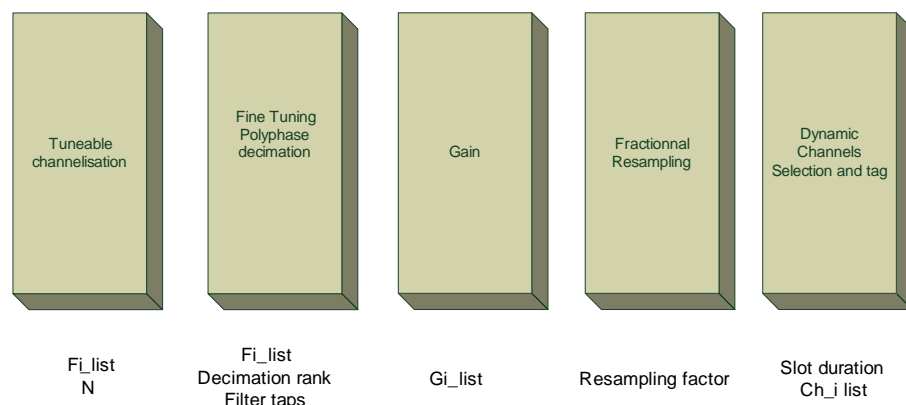


Figure 2 : Tunable channelizer

To have this agility, the channelizer implements several functions. In the first time the channelizer makes an input wideband division with decimation by N with 80dB image rejection.

Then to select the useful channel, each channel implements an independent NCO to perform fine frequency tuning with 32 bits resolution. The NCO is implemented with a Direct Digital Synthesis which has a SFDR of more than 80dB.

For all channels, it is implemented a common polyphase filter with a common integer decimation filter from 4 to 63 in steps of 1 by channel. The filter structure allows to have a filter tap number of 28 times the decimation factor of the filter, i.e. for a decimation factor of 4 we have a filter tap of 112. With this dimension we can have for an output bandwidth of 80% of the output sampling rate, a rejection outside band of 90dB with a pass band ripple less of 0.1dB.

Each channel implements independent 17 bits resolution gain as well as independent fractional resampling factor with 30 bits resolution. The resolution gain is an unsigned number which bits[6:0] are considered the fractional part and bits[16:7] are the integer part. The fractional resampler allows to have an independent decimation factor from 1 to 2 with 30 bits resolution. This independent fractional resampler can be useful for a base station in the case of phase adjustment, these errors being induced by different O.L. of terminals.

Independent tuning, fractional resampling and gain can be applied on the fly for each channel. In order to save the output bus bandwidth, an optional channel selection block allows you to select the time slots and frequency channels you want to produce.

For example, for $N=64$ channels the total decimation factor is programmable from $4*N=256$ to $63*N=4032$ in steps of 64. In this example we do not consider the fractional resampler.

Key features:

- Input real or complex on 16 bit up to 160MHz.
- $N=8$ to 1024 output channels (factory parameters).
- Independent frequency tuning with 32 bit resolution.
- Independent channel gain with 17 bit resolution, 0 to 60dB gain boost.
- Output sample rate from $F_s/(4*N)$ to $F_s/(63*N)$ by step of 1.
- Independent fractional resampler with decimation factor from 1 to 2 with 30bit resolution.
- Maximum alias-free output bandwidth of
 - $N=8$: $F_s/40$ (3.5MHz for $F_s=140$ MHz)
 - $N=1024$: $F_s/5120$ (27.34kHz for $F_s=140$ MHz)
- Filter performance with equiripple filter: 0.04dB in the passband with a rejection outside band of 90dB with an output bandwidth of 80% of the output sampling rate.

R-Interface fixed channelizer

In several applications, the frequency tuning can not be useful. In this case R-Interface proposes a fixed channelizer which allows to down convert from $N=8$ to 4096 channels in equi-space repartition.

The R-Interface core accepts real and complex data input at rate up to 190MHz.

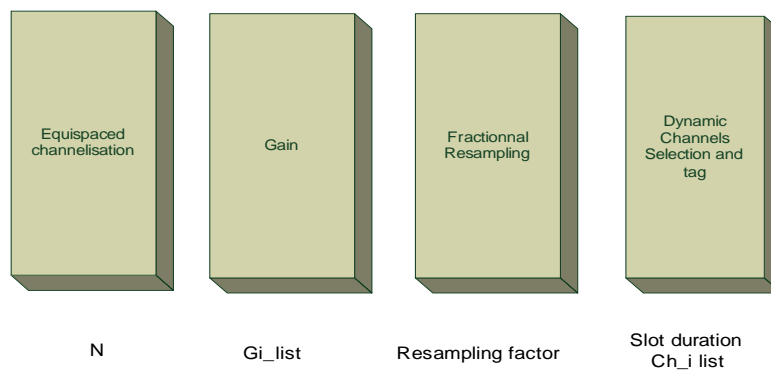


Figure 3 : fixed channelizer

The performances are the same than the tunable channelizer:

- an output bandwidth of 80% of the output sampling rate, a spurious free dynamic range of 90dB with a pass band ripple less of 0.1dB.
- a gain with 17 bit resolution.
- A fractional resampling factor with 30 bit resolution.

In order to save the output bus bandwidth, an optional channel selection block allows you to selects the time slots and frequency channels you want to produce.

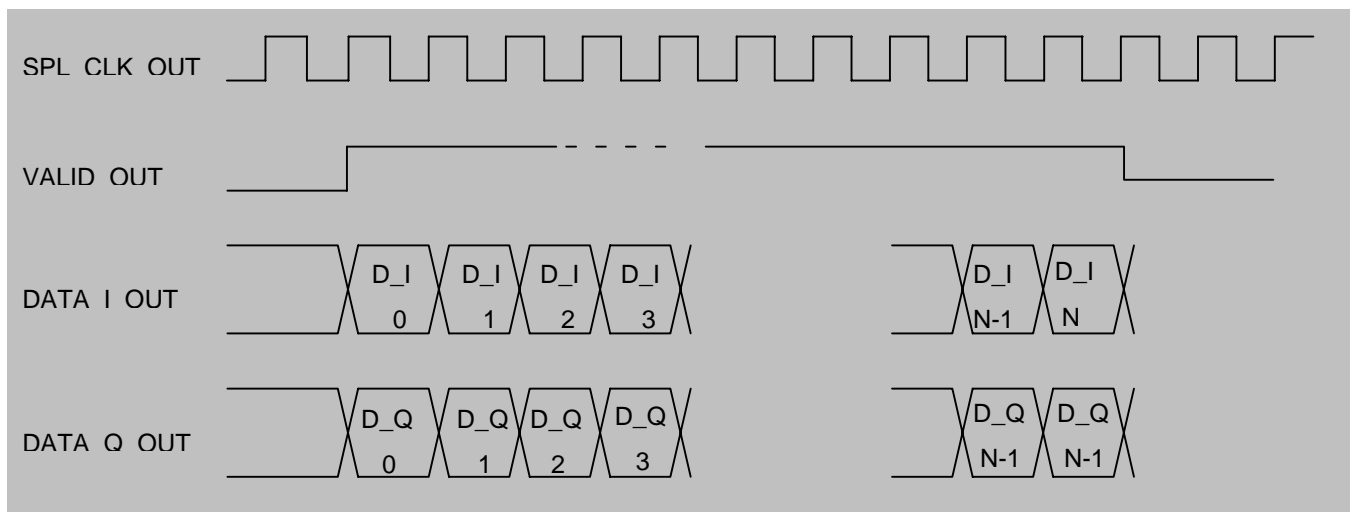
Key features:

- Input real or complex on 16 bit up to 160MHz.

- N=8 to 4096 output channels (factory parameters).
- Independent channel gain with 17 bit resolution, 0 to 60dB gain boost.
- Independent fractional resampler with decimation factor from 1 to 2 with 30bit resolution.
- Maximum alias-free output bandwidth of
 - N=8: $F_s/10$ (14MHz for $F_s=140\text{MHz}$)
 - N=4096: $F_s/5120$ (27.34kHz for $F_s=140\text{MHz}$)
- Filter performance with equiripple filter: 0.1dB in the passband with a rejection outside band of 90dB with an output bandwidth of 80% of the output sampling rate.

Data format

Data are output by burst as a double interleaved complex output data stream. One data per channel multiplexed on the same data line.



Output data format

This format can be modified on demand

Applications examples

In this section we give some examples of applications and parameters settings handled by the channelizer.

	DCS + GSM	GSM	IS-136	INMARSAT
Total bandwidth	100 MHz	25 MHz	25 MHz	34 MHz
Input sampling rate	138,62 MHz	138,666 MHz	95.846 MHz	95,846 MHz
Output sampling rate	1,083 MHz ($4 \cdot R_s$)	270,833 KHz (R_s)	93,6 KHz ($4 \cdot R_s$)	748,8 KHz ($4 \cdot R_s$)
Output Channel bandwidth	1 MHz (5 channels)	200 KHz	30 KHz	200KHz
Output Channels number	32	125	256	32
Target	Virtex 2 VP40	Virtex 2 VP50	Virtex 2 VP50	Virtex 2 VP40

Applications examples

Customization on demand.

Ressources examples

	SLICES	RAM
128 Output Channels	17000(69%)	150(47%)
256 Output Channels	18000(74%)	160(50%)
VIRTEX4 SX55	24576	320

Ressources for the tunable channelizer

	SLICES	RAM
128 Output Channels	7000(29%)	50(15%)
4096 Output Channels	9000(37%)	260(81%)
VIRTEX4 SX55	24576	320

Ressources for the fixed channelizer

Pin Description

Signal	Description	Direction
SYST_CLK	System Clock.	I
RESET	Asynchronous Hardware Reset. Active level is factory defined.	I
VALID_IN	Data is valid. Active High.	I
SPL_CLK_IN	Sample clock in. Input data are synchronous on this clock.	I
DIN_Q[M-1:0]	M bits in quadrature part of the complex input.	I
DIN_I[M-1:0]	M bits in phase part of the complex input.	I
M_ADD [AB-1 :0]	Address bus size factory defined	I
M_DATA_IN[DB-1 :0]	Microprocessor access input data bus.	I
M_DATA_OUT[DB-1 :0]	Microprocessor access output data bus.	O
IP_SEL	Chip select – Level is factory defined	I
M_WRITE	Write access – Level is factory defined	I

M_READ	Read access - Level is factory defined	I
DOUT_Q[P-1:0]	N bits in quadrature part of the complex output	O
DOUT_I[P-1:0]	N bits in phase part of the complex output	O
SPL_CLK_OUT	Sample clock out. Output data are synchronous on this clock rising edge.	O
VALID_OUT	Data out valid. Active high	O

Features and applications

- Fully synchronous design
- Up to 4096 channels proceed on one FPGA
- Up to 190 MSPS input sampling rate
- Customization and resource estimation on demand
- Multi-channels Demultiplexing and Digital Down Conversion
- Electronic Warfare (COMINT, SIGINT)
- Commercial base stations
- Spectrum analysis

Deliverables

- FPGA netlist
- Specifications include : User Guide, Test Specification, Synthesis recommendations
- Vhdl testbenches self checking
- Simulation scripts, test vectors, expected results and comparison utilities

Contact Information

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Note

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